

LOW DELAY AND AREA EFFICIENT 128 BIT CARRY SELECT ADDER USING D LATCH

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ABSTRACT:

Designing of a high speed adder is one of the most important areas of research in VLSI design. A ripple carry adder (RCA) is a simple adder and can be used to add unrestricted bit length number. But, it is not efficient to add very large bit length numbers. The main drawback is the delay that increases with the length. The carry look ahead (CLA) adder solves this problem by calculating the carry signals in advance. This adder but has area complexities. Thus carry select adder (CSLA) is proposed which is a fastest adder among the conventional adders. The modified CSLA has been developed using binary to excess-1 converter (BEC). This paper proposes the use of D-latch instead of BEC which has the advantage in terms of power, area and also delay.

Index terms: CSLA, mux, BEC, area-efficient

I. INTRODUCTION

Demand for area and power efficient high speed logic is increasing which motivates VLSI designers into new approaches. CSLA is such an adder which is efficient in terms of power, area, and speed. It alleviates the problem of carry propagation delay. Regular CSLA is composed of RCA-RCA combination. This combination generate partial sum and carry with $C_{in}=0$ and $C_{in}=1$, then the final sum and carry are selected by multiplexers. Modified CSLA was proposed in order to reduce delay and area. For this, RCA with $C_{in}=1$ is replaced by Binary to Excess-1 Converter. The basic idea of this paper is to implement D-latch instead of BEC. The decreased area, delay and power is the main advantage to replace D-latches.

II. REGULAR 128 BIT CSLA

The regular CSLA is a parallel computation which generates many carries and partial sum. Then, it is fed as input to the multiplexers. mux selects the final sum and output in accordance with the input value of C_{in} . Multiple pairs of RCA are used in CSLA structure. Each part of adder consist of two RCAs with $C_{in}=0$ and $C_{in}=1$. The RCA with $C_{in}=0$ uses half adder and full adder for $C_{in}=1$.

The regular CSLA comprises combinations of RCA in various sizes and they are divided into groups. It has 16 groups of different size RCA. The structure of RCA is simple which allows fast design time. However it is meant slow, since each adder must wait for the carry bit to be calculated from the previous adder. Group 1 contains 2 bit RCA which has only one ripple carry adder. It adds the input bits, input carry and result, sum and carry. In the following groups there are two RCA that receive same input but C_{in} as 0 and 1. The upper RCA computes sum and carry with $C_{in}=0$ and lower RCA computes sum and carry with $C_{in}=1$.

Fig1 shows the group 3 architecture of regular CSLA which has two three bit RCAs for computing partial sum and carry. Then it is fed into a 8:4 mux to retrieve the output sum and carry.

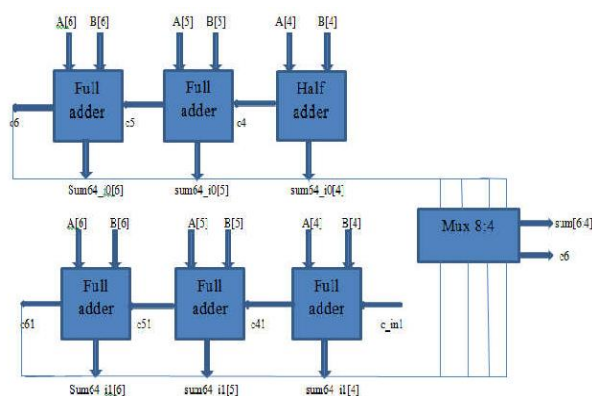


Fig1: Group 3 architecture of regular CSLA

Fig.2 shows the 128 bit regular CSLA. This is not area efficient since it uses multiple pairs of ripple carry adder. The area evaluation has to be done by counting each of the AOI gates which will be required for implementing each Logic gates.

The area evaluation is depicted in the table1. It compares the regular modified and the proposed CSLA in terms of area, delay and speed.

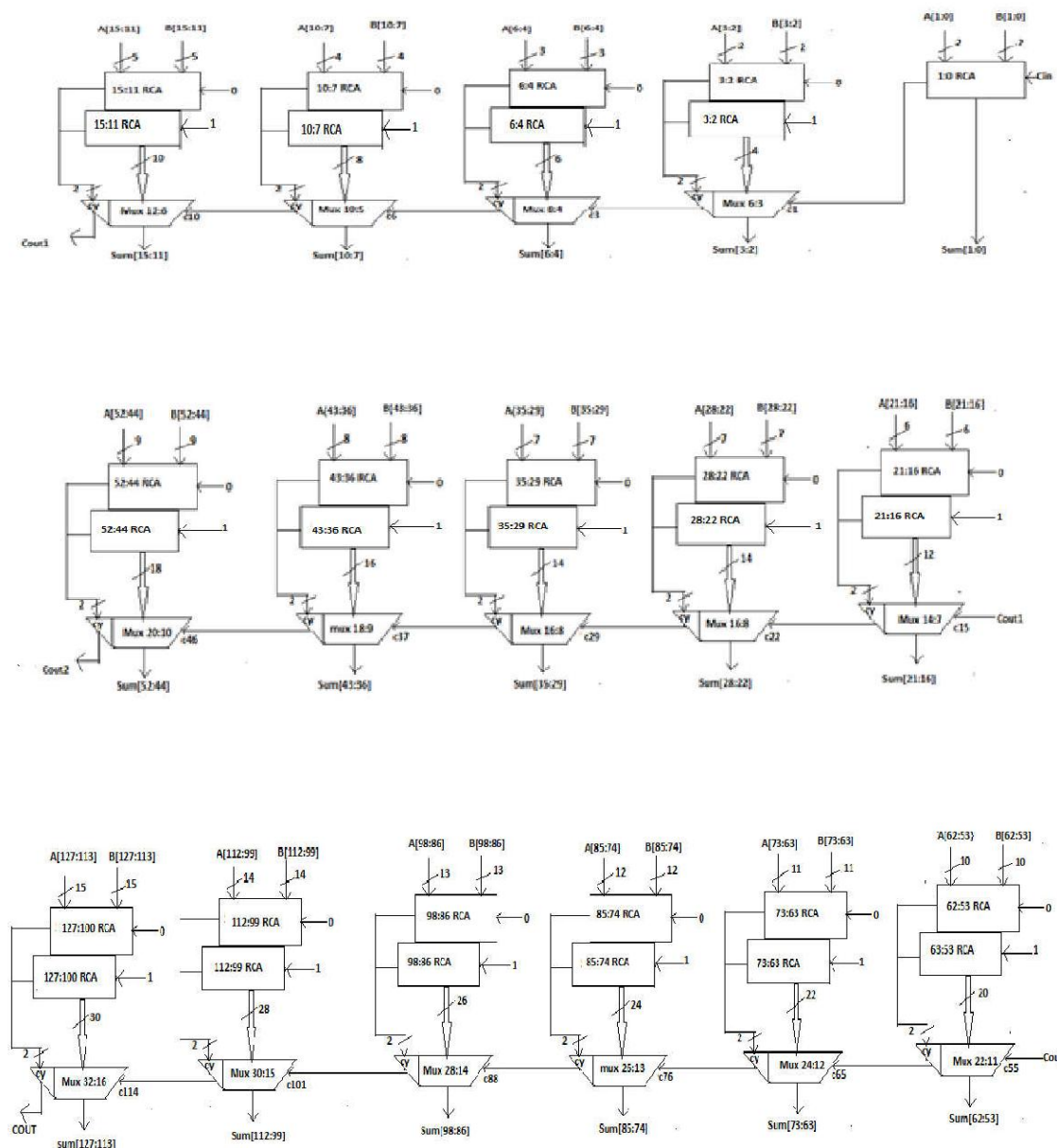


Fig 2: Architecture of 128 bit Regular CSLA

III. MODIFIED 128 BIT CSLA

The main idea of the modified 128 bit CSLA is to reduce the area and power. The BEC replaces the RCA with Cin=1 among the two available RCAs. BEC is a circuit used to add 1 to the input numbers. The circuit of BEC is shown in the fig.3. By the use of BEC logic, it is possible to reduce the significant amount of silicon area in the VLSI design. The Boolean expression for 4bit BEC are given below

$$\begin{aligned} X0 &= \sim B0 \\ X1 &= B0 \wedge B1 \\ X2 &= (B0 \& B1) \wedge B2 \\ X3 &= (B0 \& B1 \& B2) \wedge B3 \end{aligned}$$

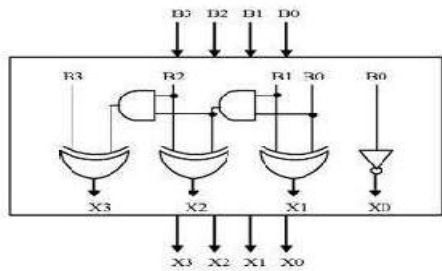


Fig.3 4bit BEC

B[3]	B[2]	B[1]	B[0]	X[3]	X[2]	X[1]	X[0]
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
.	.	.	.	.	.	.	.
1	1	1	1	0	0	0	0

Fig.4 Function table of 4 bit BEC

To replace the n-bit RCA, an n+1 bit BEC isrequired. That is, the number of bits required for BEC is 1 bit more than the RCA bits. The modified CSLA is also divided into groups with each group comprising RCA,BEC and Mux. Fig.5 shows the modified CSLA which depicts the implement of BEC in the place of upper RCA.

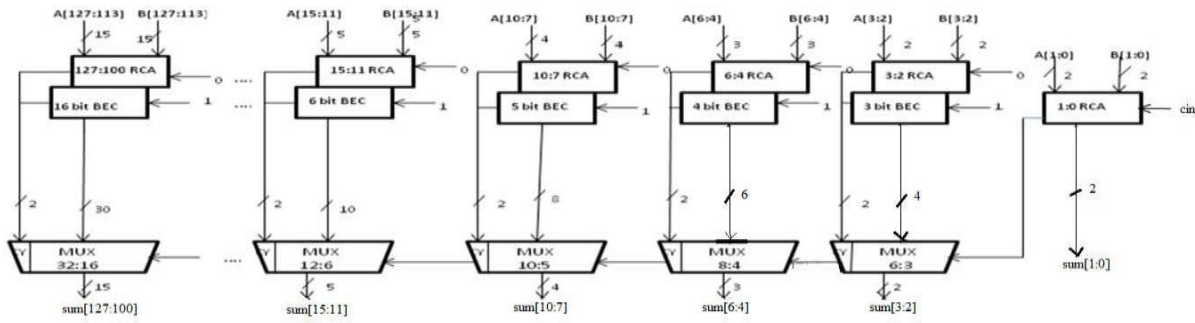


Fig.5 architecture of 128 bit modified CSLA

IV. PROPOSED CSLA USING D-LATCH

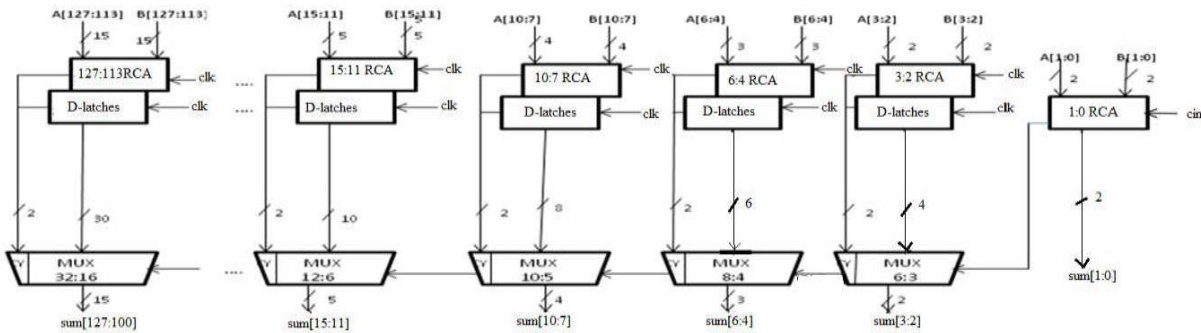


Fig.6 Architecture of proposed 128bit carry select adder

The proposed CSLA replaces the BEC add one circuit by D-latch with enable signal. Latches are those that are used to store information of one bit. They operate in accordance with the enable signal. That is, when they are enabled their output changes immediately according to the input. When the enable signal goes low, it traces the previous stage output. Fig.7 and shows the output waveform.

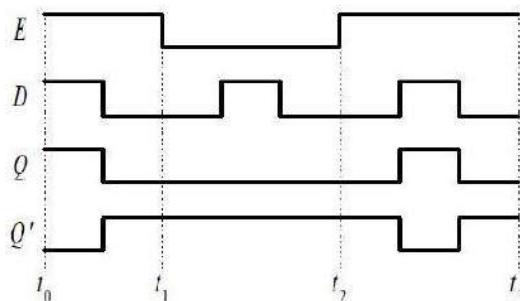


Fig.7 Timing waveform

This 128 bit adder has ripple carry adder in the upper half which works according to the enable signal. Whenever the enable signal is high, addition for carry input is performed. When the enable signal is low, the carry input is assumed as zero and sum is stored in adder itself. That is, initially when $E=1$, the output of the RCA is fed as input to the D-latch and the output of the D-latch is given as input to the mux. When $E=0$, the last state of the D input is trapped and held in the Latch and the output from the RCA is given as an input to the mux. Then the mux selects the sum bit in accordance with the input carry. The input carry acts as the selection bit to the mux. The proposed is also into 16 groups. Fig.8 shows the internal structure of group 2 of the proposed 128 bit CSLA.

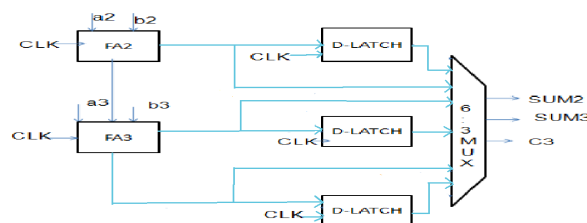


Fig.8 Group 2 structure

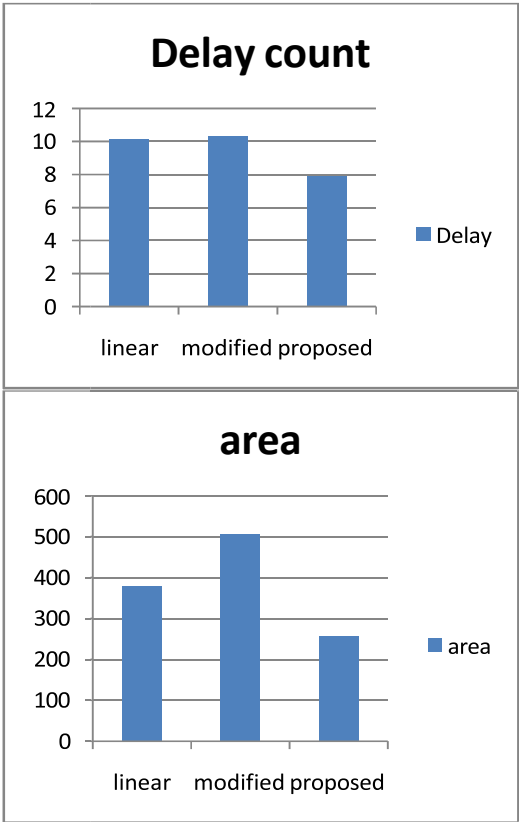
In this, when $E=0$ a_2 and b_2 are added with carry 0. Thus D- latch is not enabled. When $E=1$ addition is performed with carry 1. All the D- latches are enabled and the sum and carry are stored for carry 1. According to the input carry mux selects the actual sum and carry.

V.COMPARISON

The proposed CSLA mainly involves in the reduction of the delay, area and in the enhancement of the speed. The table.1 shows the comparison of the proposed CSLA with that of the regular and modified CSLA. It is seen that the carry select adder using D-latch has less delay and area.

Table.1 Comparison of regular modified and proposed CSLA

Parameter	Regular CSLA	Modified CSLA	Proposed CSLA
Delay(ns)	10.186	10.305	7.895
Time for Real time computation (ns)	26.00	22.00	19.00
Time for CPU time computation (ns)	25.40	21.87	18.88
Area (No of gates)	380	506	256



VI. SIMULATION RESULT

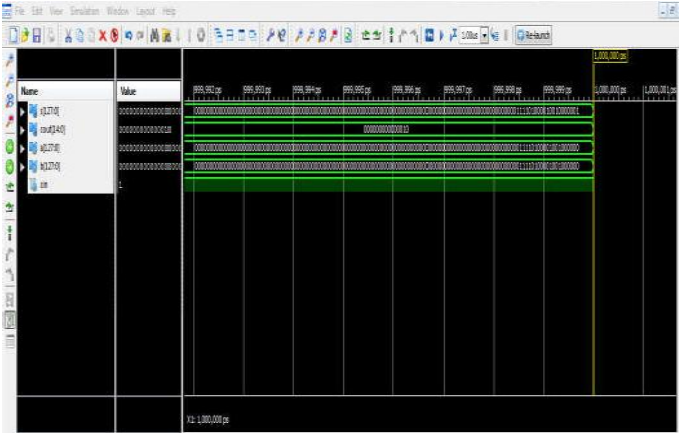


Fig.9 128 bit Regular CSLA

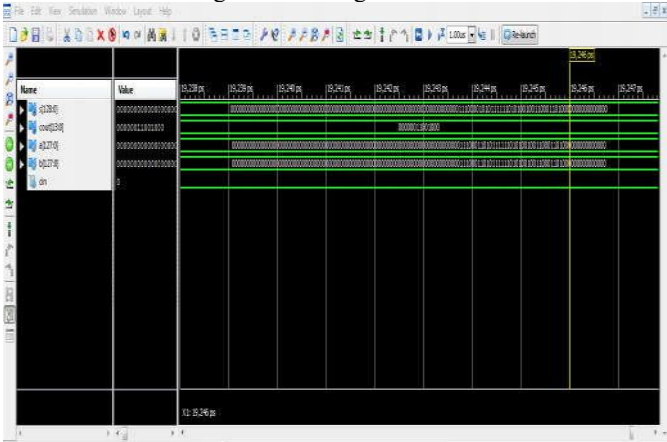


Fig.10 128 bit Modified CSLA

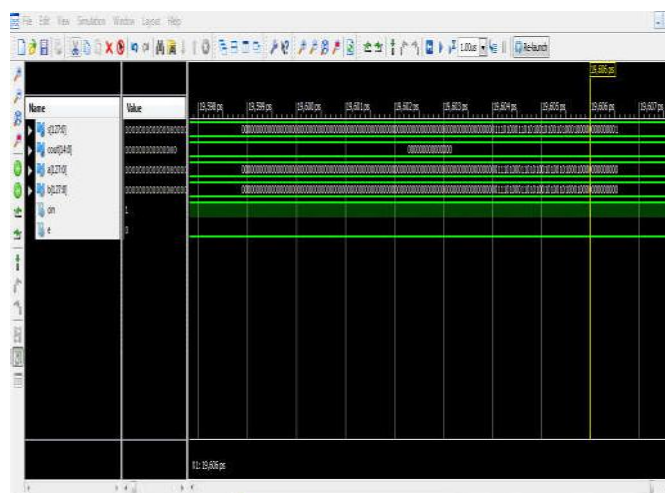


Fig.11 128 bit proposed CSLA

VII. CONCLUSION

This paper compares the regular, modified and the proposed CSLA which is implemented using D-latch. The proposed CSLA is a simple approach to enhance the carry select adder in terms of area and delay. Finally compared result shows that the carry select adder using D-latch will have less delay and it is area-efficient. This CSLA is also efficient for hardware implementation. The future work may be carried out with a 256bit carry select adder which would be interesting to test.

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