Current transport in SiO_2 films grown by thermal oxidation for metal-oxide semiconductor

Marwa Abdul Muhsien, Ibrahim R. Agool, A. M. Abaas and K. N. Abdalla

Department of Physics, College of Science, Al Mustansiriyah University, Baghdad, Iraq.

Electrical properties of Al- SiO_2- P-Si were studied; SiO_2 films with different thickness were grown by thermal oxidation (dry oxygen) on p- type silicon surface. I-V characteristic of th ese capaci to rs w ee measu red at di fferen t temp eratu re (300-100) K with different oxide thickness. C-V measurement for capacitors with thickness (20-50) nm where studied at (100) kHz. As a conclusion the current transport mechanism in the capacitors was believed to be space charge lirhited current at temperature between (300-200) K, at low temperature field ionization happen. Interface states and doping density also calculated from C-V measurement.

Keywords: Thermal oxidation, metal-oxide, semiconductor, temperature, density,C-V measurement.

INTRODUCTION

Due to the various applications of insulators films: to serve a mask against implant or diffusion of dopant into semiconductor, to provide passivation, to isolate one device from another and to act as component in MOS structure (Marwa and Hassan, 2009). Several techniques for forming oxide layers have been developed such as thermal oxidation, wet anodization vapor phase, plasma ionization or oxidation (Tsung-Han et al., 2007). Electronic industry needs requires thin, high quality insulating films for gate dielectrics and storage capacitors and memory devices in very large scale integrated (VLSI) circuits. Thermal SiO_2 films has been most widely used in integrated ciscuits due to superior insulating of SiO_2 films, thermal stability, a stable SiO_2/Si interface and simple processing requirements (Morgan and Board, 1985).

Experimental Procedure

Metal – Oxide – Semiconductor capacitors were fabricated on p- type <100>- oriention silicon, slices were cleaned in both organic and inorganic solvents: first ultra sonically cleaned by trichloroethylene (TCE) solution, immersed in acetone and isopropanol (IP) and dipped in deionized water silicon slices chemically polished in a 1: 10 HF: H_2O solution, rinsed in deionized water and immediately oxidized in dry oxygen at temperature (800, 850, 900) ˚C for (30 min). For ohmic contact oxide from back of slices was removed by hydroflouric acid. Aluminum metal thermal evaporated on aback slices and annealling in vacuum tube at temperature (400 ˚C) for (30 min). To complete fabricating MOS- capacitors field plates aluminum dots (area = 1.767×10^{-2} cm^2) evaporating through metal mask on to SiO_2 films, individual capacitors were scribed and mounted in TO5-headers.

Theory

Current-voltage measurements of direct current leakage through MOS -capacitors were carried out using digital multimeter type 177. For measuring at different low temperature used cryostat. Figure (1) show current – voltage for MOS- capacitors at (300 K) is bulk controlled at (0.6) volt and figures (2, 3, 4) show typical logarithmic current – voltage plots for MOS- capacitors and from logarithmic plots show sharp increase of current leakage with increase applied bias according to relation ($I\alpha V^m$) where m from (3~9), with increasing applied bias this relation don't satisfy and show a break in curve and current become proportional to square voltage ($I\alpha V^m$)

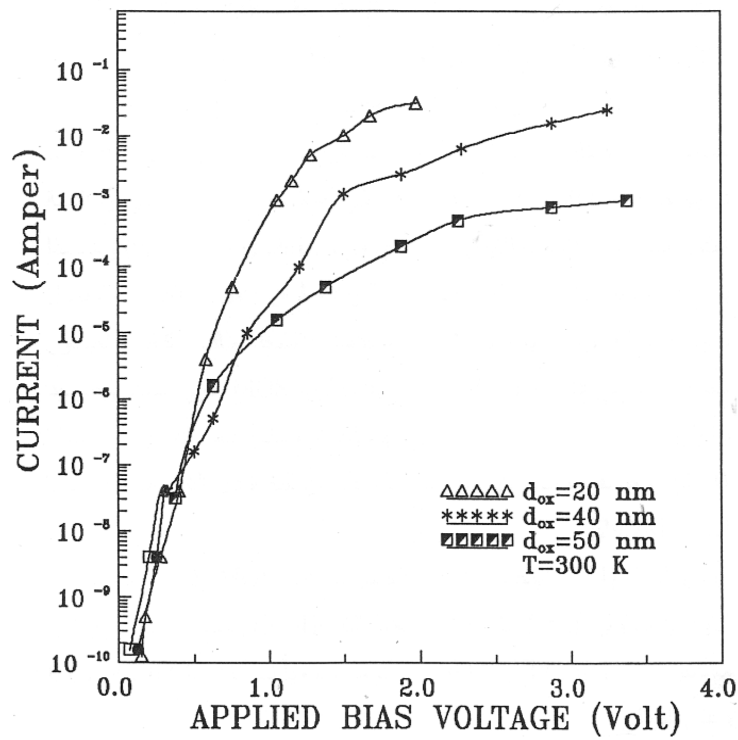

Figure 1. Current-Voltage characteristics for Si films- SiO_2- Al capacitors at room temperature.

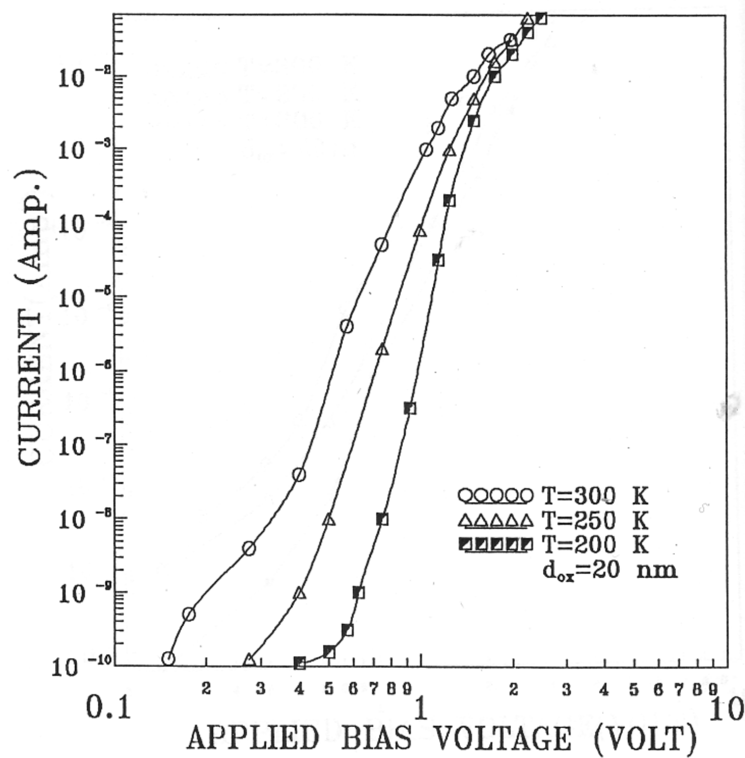

Figure 2. Log I against Log V plot for SiO_2 films with thickness 20 nm at low temperature.

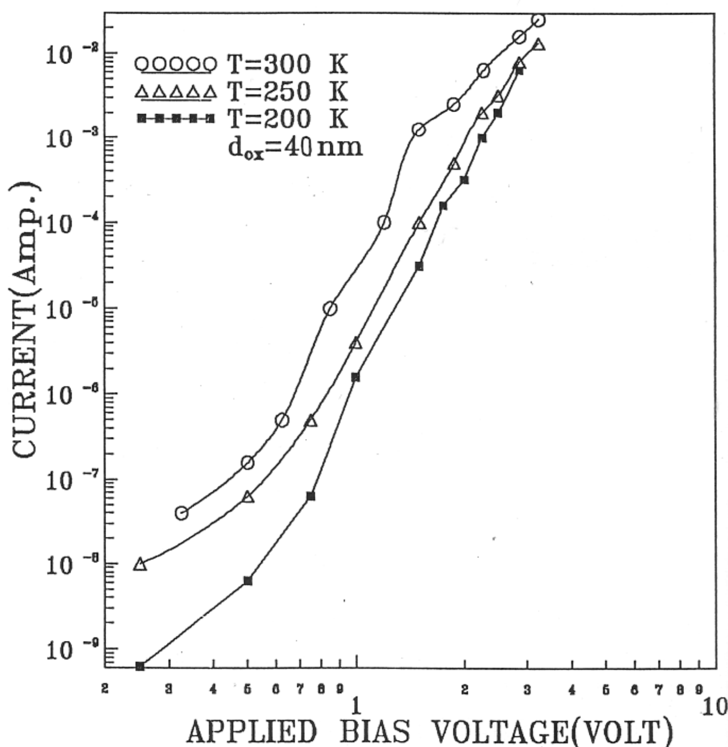

Figure 3. Log I against Log V plot for SiO_2 films with thickness 40 nm at different temperature.

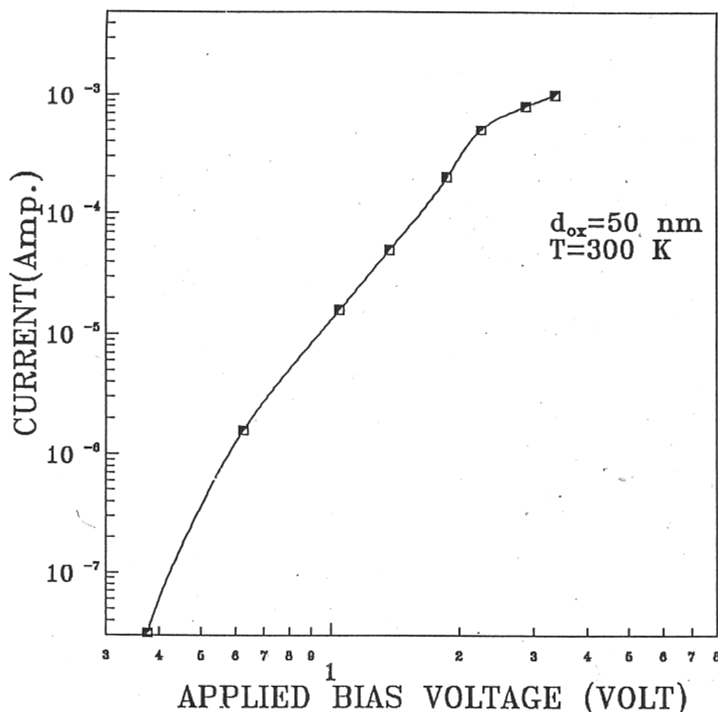

Figure 4. Log I against Log V plot for SiO_2 films with thickness 50 nm at room temperature.

which is characteristics of space charge limited current (SCLC) with shallow traps. In (1955) Rose (Sze, 1987) indicate space charge- limited current in defects insulators, Rose show that the insulator contain traps, the

Table 1. Experimentally parameters for MOS capacitors from I-V measurements.

Oxide thickness (nm)	20	40	50
V_{TFL} volt	1.15	1.5	2.25
N_t/cm^2	6×10^{17}	2.6×10^{17}	1.99×10^{17}
$\theta = n_i/n_t$	4.6×10^{-18}	1.8×10^{-18}	1.2×10^{-18}
E_t (eV)	0.53	0.58	0.55

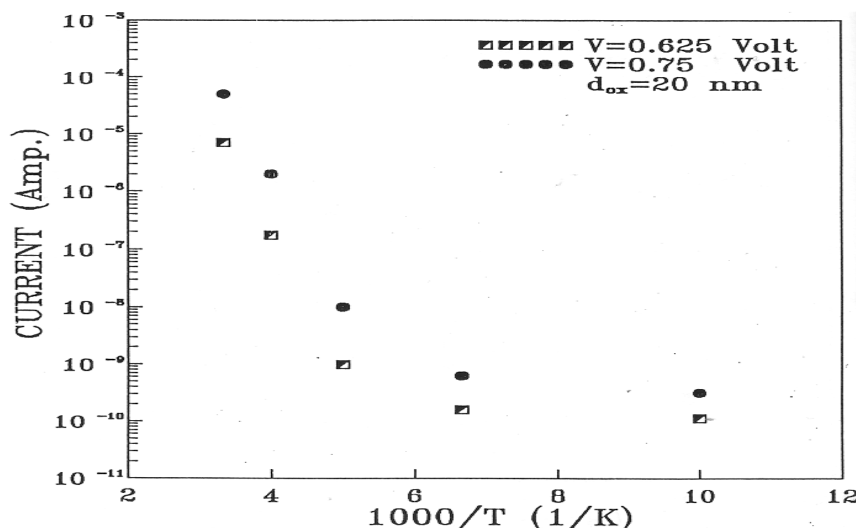

Figure 5. Logarithmic plots of current against 1000/T for Si- SiO_2 – Al films capacitor with oxide thickness 20 nm.

current in insulators is less than trap – free insulator due to traps capture a large fraction of injected electron in insulator by applied bias. By considering, the insulator contains density of shall traps (N_t) (shallow traps are defined as being as at least (K_BT) above Fermi level, and traps positioned an energy (E_t) below the conduction band of insulator , the ratio of free – to – trappeed charge (θ) is:

$$\theta = \frac{N_c}{N_t}\exp\left(-\frac{E_t}{K_B T}\right)$$

……………………..…………………………………………… ……. (1)

Where (N_C) density of state, (K_B) Boltzman constant, (N_t) traps density. To in corporate the effect of shallow traps in insulators the density of current of space – charge limited indicate in equation (2) Where (ε_{ox}) dielectric constaint, (ε_o) space permittivity, (μ) mobility of carrier, (d) insulator thickness. Lampert (Paihung and Charles, 1986) has calculated the complete current – voltage curve of space charge limited current and show it consist of four discrect regions, at low applied bias the injected carrier density (n_i) is less than free carrier density (n_o) ohmic conductivity will predominate. When the injected carrier density is greater than free carrier density the current become space – charge limited but is modified by traps in the insulator eq. (2). At voltage (V_{TFL}) the current increase rapidly due the traps will become filled and further injected charge then exist as free charge in the conduction band into current. The voltage at which the traps will becames filled is given by eq. (3) and by using eq (1) and (2) and (3) we calcaluted the density of traps, the ratio free to traped carriers (θ) and energy of traps (E_t), these value indicate in table (1) and well agreement with either worker (Sze and Kwok, 2007).

$$V_{TFL} = \frac{eNtd^2}{\varepsilon\varepsilon_{ox}}$$

……………………………………………………………..…… ………..… (3)

Some authors indicate that sharp increase in current due to trap emptying arising from the Poole – frenkel effect (HER et al., 1987; Madan et al., 1980).

$$J = BE\exp\frac{\sqrt{e^3 E/\pi\varepsilon_{ox}\varepsilon_o} - \Phi_{PF}}{K_B T}$$

……………………………………………………………….. (4)

Where (Φ_{PF}) is the potential barrier of traps, (B) constant, the absence of linear region in plot of log I/E against E1/2 indicate that Poole – Frenkle effect is inresbonsible of sharp increase of current. This enhacement the sharp increase due the trap filled with carrier charge. In figure (5), (6) a plot of leakage current

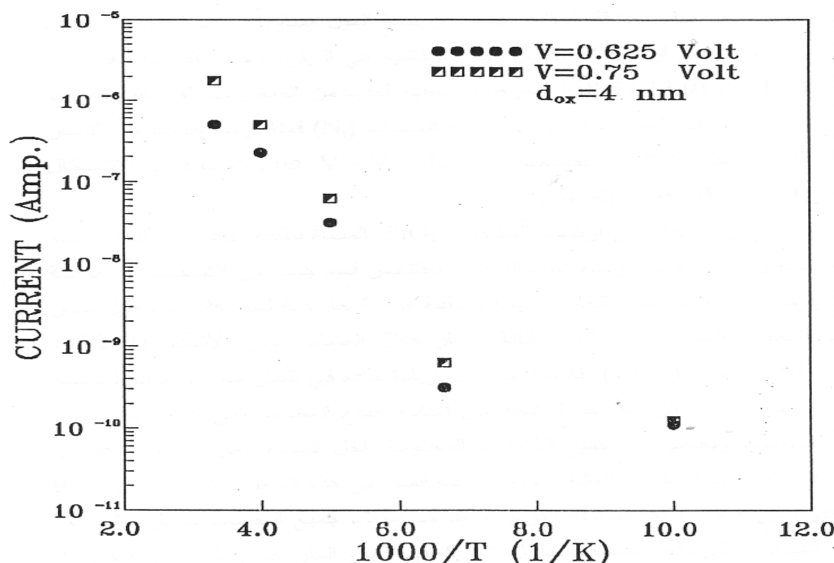

Figure 6. Logarithmic plots of current against 1000/T for Si- SiO_2 – Al films capacitor with oxide thickness 40 nm.

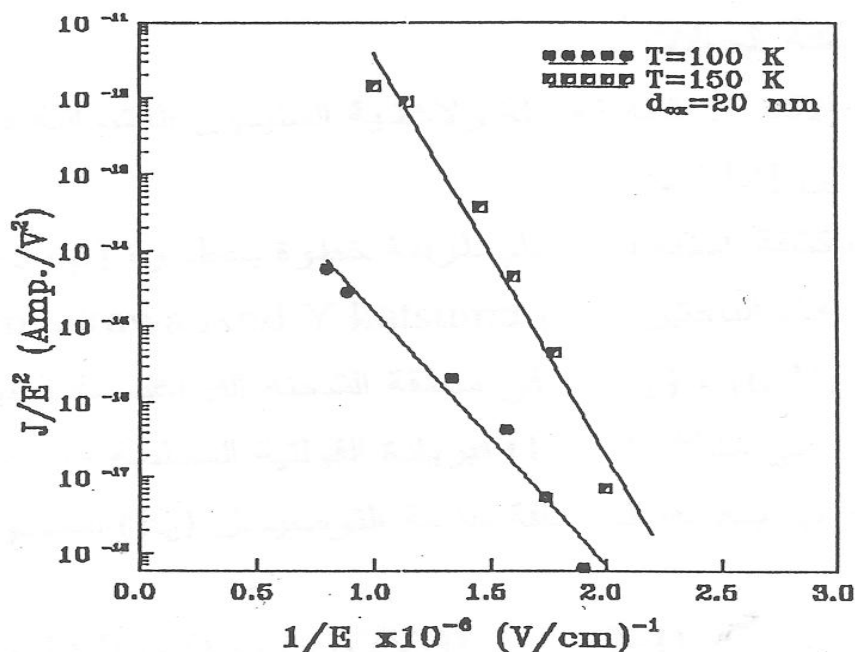

Figure 7. Field ionization plot of J/E^2 for oxide thickness 20 nm.

V_s 1/T is shown and the activation energy calculated from the slope 0.44 eV, 0.2 for SiO_2 films (20, 40) nm respectively. At temperature below (200) K the current become nearly indepent on temperature. This behavior is similar to ather insulator as Si_3N_4 films on Si (Spparal and Herman, 1995). The current is due to field ionization of trapped electrons from the traps. This is tunneling process essentially independent of temperature.

$$J = CE^2 \exp\left(-\frac{B}{E}\right)$$ ……………………………………………………………………. (5)

By plotting I/E^2- Vs- 1/E in figures (7), (8) indicate a linear relation at high field. From the slope of these figs. We found potential depth of traps ≈ 0.3 eV which

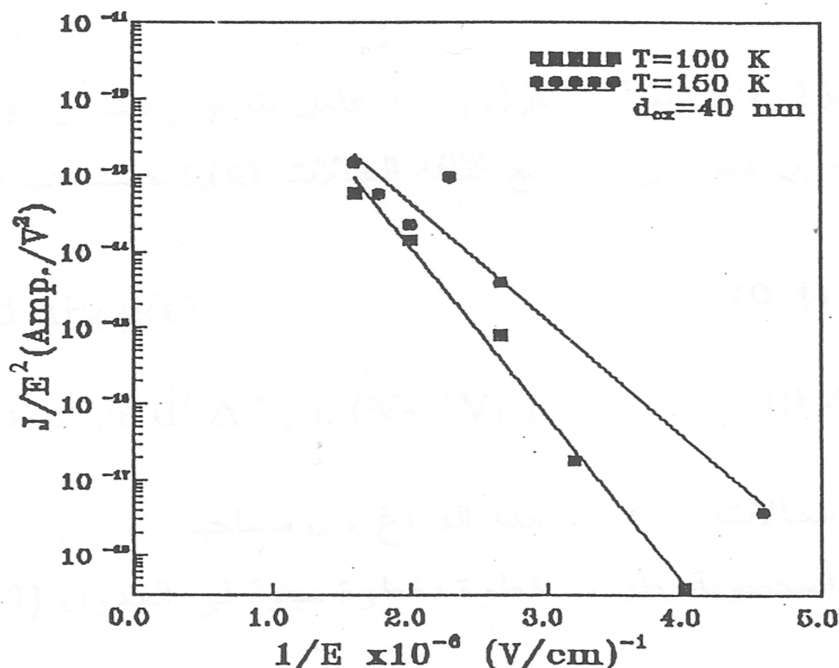

Figure 8. Field ionization plot of J/E^2 for oxide thickness 40 nm.

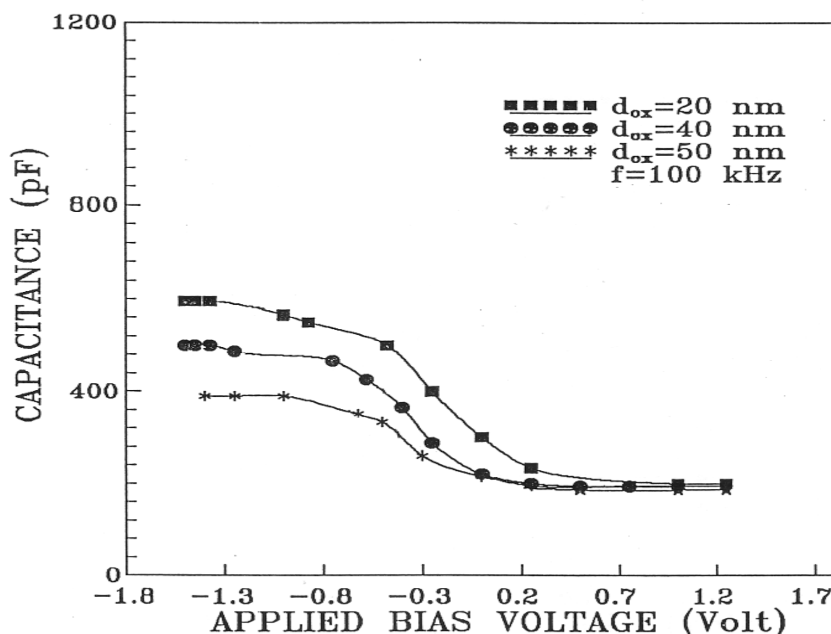

Figure 9. Capacitance-Voltage characteristics of Si films- SiO_2- Al capacitors.

agreement with these values calculated by space- charge limit current.

Capacitance – Voltage

The oxide coated semiconductor is an integral part of many recent devices. These include the silicon planar, MOS transistors and charge coupled devices. Successful operation of devices is largely depending on the quality of oxide – semiconductor interface. The C-V characteristics of AL/SiO_2/p-Si capacitors with different oxide thickness at (100) kHz is shown in figure (9) measuring by LCR multi frequency HP 4274, according to the following equation (Nicollian and Brews, 1982).

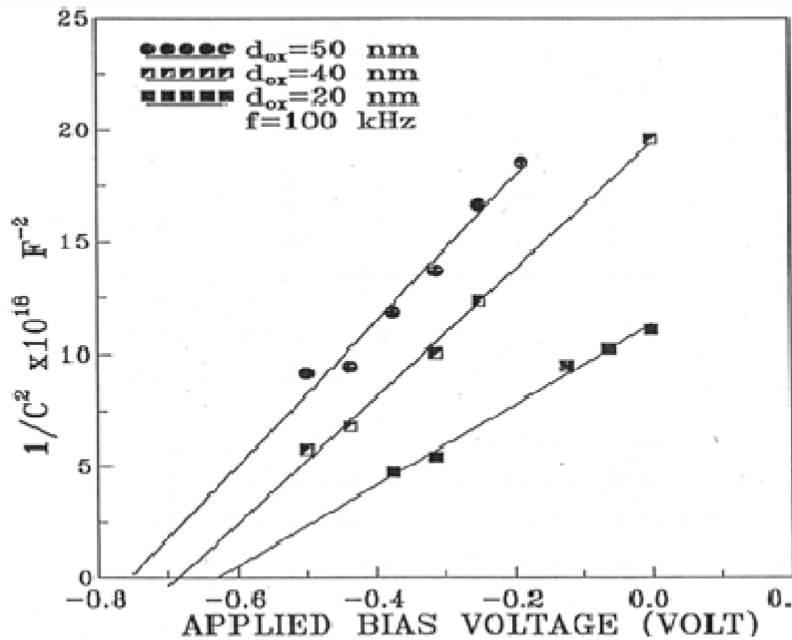

Figure 10. Reciproical square capacitance vs. applied voltage behavior.

$$C = \frac{C_{OX}(C_S + C_{SS})}{C_{OX} + C_S + C_{SS}}$$ ………………………..……………………………………………… (6)

Where (C) is the capacitance of structer, (C_{ox}) capacitance of oxide, (C_{ss}) capacitance of surface states and (C_s) capacitance of space charge region,the form of this equation indicate that the oxide capacity is in series with parallel combination of the surface state capacity and space charge capacity,if the frequency of applied voltage is made high enough, the surface state capacitance in equation (7) approach zero and the measured capacitance is just oxide capacitance and space charge capacitance in series, for this case we can write equation (6) as

$$C = \frac{C_{OX}\,C_S}{C_{OX} + C_S}$$ ……………………………………………………………..……………….. (7)

The oxide capacity is constant, and equal to maximum measure capacitance in accumulation region, the charge in capacitance can rise from the charge semiconductor capacitance with charge of applied voltage due to the change in the space charge region width, as shown in expermental C-V curves, when applied bias became less negative this leads the capacitance have a minmum value and saturated at this value. The space charge capacity is depending on the response of minority carriers in inversion region. In this region the capacity is limited by ability of minority carriers to follow the applied field at the test frequency .The flat band voltage (V_{fb}) where determined according to Lehovec (Neamen, 1992), who differentiate the following expression to calculate the surface states density

$$D_{it} = \frac{(C_{OX} - C_S)C_S}{3\left(\frac{\partial C}{\partial V}\right) e K_B T} - \frac{C^2{}_{OX}}{(C_{OX} - C)e^2}$$ ….. (8)

The values of C and are taken from expermintal C-V curves at flat band voltage, other method was used to calculate the surface states, this value indicate in Table (2) (Alferov, 1987), the reciprocal square capacitance verus applied voltage is shown in figure (10), the curve indicate the plot yield a straight line, the acceptor density can calculate from slope of the curves and by using equation for C-V profiling of semiconductor devices.

$$Na = \frac{2}{eA^2 \varepsilon_0 \varepsilon_{OX} (dC - \frac{2}{dv})}$$ ………………………………………………………………..…… (10)

CONCLUSIONS

1. The conduction mechanism in $AL/SiO_2/Si$ devices is space charge limited current, the curve of log(1) verese log (V) indicate a sharp increase in the current due to traps capture the injected carriers until the traps filled, after this point the current become proportional for square voltage (JαV2)
2. At very low temperatures between (150-100) K the mechanism is field ionization of trapped charges.
3. The shift in (V_{fb}) value which been obtained from C-V

characteristics due to contains oxide films positive charges, C-V curves indicate the capacitance in inversion region depend on a test frequency due to the minority carriers response time.

REFERENCES

Marwa A, Hassan A (2009). Construction and characterization of MIS Heterojunction devices. MSc (Al-Mustansiriya University), p.31.
Tsung-Han T, Jun-Rui H, Kun-Wei L, Chin-Wen H, Wei-Chou H, Huey-Ing C, Wen-Chau L (2007). Improved Hydrogen-Sensing Properties of a Pt/SiO_2/GaN Schottky Diode"Electrochemical and Solid-State Letters, Vol.10, No. (12), p. J158-J160.
Morgan DV, Board K (1985). An introduction to semiconductor microtechnology, John Wiley and Sons.
Sze SM (1987). VLSI technology MC Graw-Hill Book Company.
Paihung P, Charles S (1986). J. Electrochem. Soc.; Solid State Science and Technology, Vol. 133, No. 1171.
Sze SM, Ng Kwok K (2007). Physics of semiconductor devices, 3rd Edition.
HER, RHW (1987). "Metal- Semiconductor contacts" Oxford university press, New York.
Madan A, Mgill J, Czubatyj W, Yang J, Ovshinsky SR (1980), Appl. Phys. Lett, Vol. 37, No. (825).
Spparal B, Herman G (1995). Physics of semiconductor, New York.
Nicollian EH, Brews JR (1982). MOS physics and technology, Murray Hill, New Jersey.
Neamen DA (1992). Semiconductor physics and devices basic principles, Irwin.
Alferov IZH (1989). "Semiconductor heterostructures physical processes and applications" Printed in RSSA.